REMARKS/ARGUMENTS

The Final Office Action of October 19, 2007 has been carefully reviewed and these remarks are responsive thereto.

This Amendment is being submitted with a Request for Continued Examination filed concurrently herewith.

Claims 1, 6, 9, and 11-13 have been amended to more clearly recite the features claimed therein. Support for the amendments to claims 1, 6, 9, and 11-13 can be found, for example, at page 2, lines 27-31 and page 9, lines 3-5 of the specification. No new matter has been added, and entry of the amendments to claims 1, 6, 9, and 11-13 is respectfully requested.

Claims 2, 3, 5, 7, 8, and 10 have previously been cancelled.

Thus, claims 1, 4, 6, 9, and 11-13 are pending.

Review and reconsideration of the above-identified application are respectfully requested.

Claims 1, 4, 6, and 9

In the Office Action, claims 1, 4, 6, and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,547,849 to Louie et al. (Louie) in view of U.S. Patent No. 6,128,311 to Poulis et al. (Poulis). This rejection is respectfully traversed.

Claims 1 and 6 are the only independent claims pending. Applicants respectfully submit that neither Louie nor Poulis, alone or in combination, describes all of the features recited in claims 1 and 6 herein.

Louie describes an interface between a "master" microprocessor and a "slave" coprocessor which share a memory address bus and a data bus connected to a main memory. Louie at col. 1, lines 57-60. As described in Louie at col. 3, lines 1-47 and as shown in FIG. 1, the microprocessor of Louie comprises a bus unit 200, an address unit 206, an execution unit 204, and an instruction unit 202. The microprocessor is connected to a coprocessor 207 by means of a parallel bus interface having address line 400, data line 406, and COACK# line 402 and COREQ line 404.

The Examiner reads the microprocessor of Louie as describing the central IC and the coprocessor of Louie as describing the peripheral IC recited in the claims herein. See Office Action at pp. 3-4. The Examiner further appears to assert that the "transfer signal" recited in the claims is described by one or the other of the "COREQ" signal and the "COACK#" signal described in Louie. See Office Action at p. 4. Applicants respectfully submit, however, that neither the COREQ signal nor the COACK# signal described in Louie describes the "transfer signal" as recited in claim 1 or claim 6 herein.

As seen in FIG. 1, the COREQ signal is sent from coprocessor 207 to the microprocessor (which, as noted above comprises address unit 206, execution unit 204, instruction unit 202, and bus unit 200). Thus, the COREQ signal is sent ***from*** the peripheral IC ***to*** the central IC, exactly the opposite as the transfer signal recited in the claims, which comprises a signal from the central IC to the peripheral IC. Consequently, the COREQ signal of Louie does not describe the transfer signal recited in the claims.

The COACK# signal also does not describe the transfer signal recited in the claims. The only function of the COACK# signal described in Louie is to acknowledge a request from the coprocessor. See Louie at col. 2, lines 13-16 and 31-33; Table 7 at col. 7, lines 19-20; 54-57; and col. 24, lines 13-17. This is very different from the transfer signal recited in the claims which "[triggers] the transferring of the buffered operating parameter to the working register wherein the buffered operating parameter becomes active in a working process of the peripheral IC." In addition, the transfer signal as recited in the claims transfers the buffered operating parameter from a preregister of the peripheral IC to a working register, also in the peripheral IC. The transfer signal does not relate to a transfer of data from the central IC to the peripheral IC, in contrast to either the COREQ or the COACK# signal described in Louie, which relates to a transfer of data between the master microprocessor and the slave coprocessor in response to a request from the coprocessor. See Louie at col. 1, line 63 to col. 2, line 32.

Poulis describes a method and apparatus for interconnecting a master processor and a coprocessor via a serial bus. Poulis, Abstract, lines 1-14. Poulis further describes a serial bus interface for performing a serial to parallel and a parallel to serial conversion for exchange over a serial bus. Poulis, at col. 4, lines 29-31. Poulis does not, however, describe a method or device in which a transfer signal between a coprocessor and a master processor "[triggers] the

transferring of the buffered operating parameter to the working register, wherein the buffered operating parameter becomes active in a working process of the peripheral IC" as recited in claims 1 and 6 herein.

Poulis thus does not remedy the deficiency of Louie noted above with respect to claims 1 and 6. Therefore, the combination of Louie and Poulis does not describe all of the features recited in claims 1 and 6 as presented herein, and withdrawal of the rejection of independent claims 1 and 6 and allowance are respectfully requested.

In addition, claim 4 depends from claim 1 and claim 9 depends from claim 6. Applicants respectfully submit that these dependent claims also are allowable over the combination of Louie and Poulis because of their respective dependence on allowable base claims 1 and 6, and further because of the additional inventive aspects recited therein. Withdrawal of the rejection of claims 4 and 9 and allowance are respectfully requested.

Claims 11-13

In the Office Action, claims 11-13 were rejected under 35 U.S.C. § 103 as being unpatentable over Louie and Poulis as described above in view of U.S. Patent No. 7,120,427 to Adams et al. (Adams). This rejection is respectfully traversed.

Claims 11-13 depend, directly or indirectly, from claim 6. As noted above, claim 6 is allowable over the combination of Louie and Poulis. Adams describes a radio integrated circuit such that one or more characteristics of the radio integrated circuit are modifiable by programming a programmable bias supply. See Adams at Abstract and at col. 2, lines 26-37. Adams does not, however, describe a device in which a transfer signal from a central IC to a peripheral IC "[triggers] the transferring of the buffered operating parameter to the working register, wherein the buffered operating parameter becomes active in a working process of the peripheral IC" as recited in claim 6 herein.

Adams thus does not remedy the deficiency of Louie and Poulis with respect to claim 6. Because claim 6 is allowable over the combination of Louie, Poulis, and Adams, claims 11-13 which depend from claim 6 also are allowable over Louie, Poulis, and Adams because of their dependence on an allowable base claim and also because of the additional inventive features

recited therein. Withdrawal of the rejection of claims 11-13 and allowance are respectfully requested.

CONCLUSION

All rejections having been addressed, Applicant respectfully submits that the present application is in condition for allowance with claims 1, 4, 6, 9, and 11-13, and respectfully solicits prompt notification of the same. However, if for any reason the Examiner believes the application is not in condition for allowance or there are any questions, the Examiner is requested to contact the undersigned at 609-734-6440.

Respectfully submitted,
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Date

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